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Notes:

1. Untranslatable words are replaced with asterisks (***).
2. Texts in the figures are not translated and shown as it is.

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FULL CONTENTS

[Claim(s)]

[Claim 1]A semiconductor device comprising:

{100} sides and four peripheral sides are provided with a semiconductor substrate which has {110} sides, and a main table side, [a cross line of {111} sides of this semiconductor substrate, and said main table side] The 1st conductive layer it existed in said four peripheral sides in parallel or perpendicularly, and a slot where an inside was set as {100} sides 4 round was formed in a main table side of said semiconductor substrate, and was formed over at least one inside of this slot.

An insulating layer formed on at least one inside of this 1st conductive layer, and the 2nd conductive layer formed in the upper surface of this insulating layer.

[Claim 2]A semiconductor device with which it is a semiconductor device, {100} sides and four peripheral sides consisted of {110} sides in a main table side of said semiconductor substrate, and said slot type capacitor was formed in a slot on the square pole form where an inside consists of {100} sides the 4 round, comprising:

A semiconductor substrate which has a main table side and four peripheral sides.

A MOS type field effect transistor and a slot type capacitor which were formed on a main table side of this semiconductor substrate.

[Claim 3]Are a semiconductor device characterized by comprising the following, and a main table side of said semiconductor chip consists of {110} sides, and {100} sides and four peripheral sides, [said MOS type field effect transistor] A semiconductor device with which said slot type capacitor was formed in a slot on the square pole form where those four peripheral sides consist of {100} sides including an active region which extends in the direction which intersects perpendicularly with a gate electrode prolonged in parallel or the right-angled direction in four peripheral sides of said semiconductor chip, and this gate electrode.

A semiconductor chip which makes a rectangular parallelepiped.

A MOS type field effect transistor and a slot type capacitor which were formed on a main table side of this semiconductor chip.

[Claim 4]A main table side is a semiconductor chip in which {100} sides and four peripheral sides have {110} sides, A semiconductor device with which a slot type

capacitor is formed on this semiconductor chip, this slot type capacitor has the slot where an inside was set as {100} sides 4 round, and a cross line of {111} sides of said semiconductor chip and said main table side exists in a main table side of said semiconductor chip in parallel or perpendicularly.

[Claim 5] A semiconductor substrate which has a slot which is formed in a depth direction of a substrate from a main table side, four peripheral sides, and said main table side, and has an inside 4 round, One pair of impurity ranges formed so that a field of a semiconductor substrate in alignment with an inside of said slot might be made into channel regions, A MOS type field effect transistor which has gate dielectric film formed on said channel regions, and the gate electrode which is on said gate dielectric film and was formed over an inside of said slot, A semiconductor device, as for whose {100} sides and four peripheral sides, {110} sides and a 4-round inside consist of {100} sides in a preparation and said main table side.

[Claim 6] A manufacturing method of a semiconductor device characterized by comprising the following.

A process of forming a slot where an inside was set to a semiconductor wafer in which a main table side has {110} sides the 4 round in {100} sides.

A process of forming the 1st conductive layer over at least one inside of this slot.

A process of forming an insulating layer on at least one inside of this 1st conductive layer.

A process which carries out dicing of said semiconductor wafer to the upper surface of this insulating layer along the direction of a cross line of a process of forming the 2nd conductive layer, and said main table side and {111} sides of said semiconductor wafer and in which those four peripheral sides form a semiconductor chip which has {110} sides.

[Claim 7] A plane direction setting process are characterized by comprising the following of setting a semiconductor wafer as a predetermined plane direction, A manufacturing method of a semiconductor device provided with a process of forming a memory device which has a MOS type field effect transistor and slot type capacitor in said semiconductor wafer, and a process of carrying out dicing of said semiconductor wafer to a semiconductor chip which has a main table side and four peripheral sides.

A process of forming in a main table side of said semiconductor wafer a slot where an inside was set as {100} sides the 4 round.

A process of forming an MOS field-effect transistor in a main table side of said semiconductor wafer.

A process of forming a capacitor over at least one inside of said slot.

A process of manufacturing a semiconductor chip which carries out dicing of said semiconductor wafer along the direction of a cross line of {111} sides of said semiconductor wafer, and said main table side and in which the four peripheral sides have {110} sides.

[Claim 8] A method characterized by comprising the following of manufacturing a semiconductor device provided with a MOS type field effect transistor on a semiconductor wafer which has a main table side of {100} sides.

A process of forming in a main table side of said semiconductor wafer a slot where an

inside was set as { 100 } sides the 4 round.

A process of carrying out the ion implantation of the impurities to an inside of said slot, and forming a source/drain area, and a process of forming gate dielectric film by thermal oxidation on an inside of said slot.

A process of forming a gate electrode on said gate dielectric film by an inside of said slot.

A process which carries out dicing of said semiconductor wafer in the direction of a cross line of { 111 } sides of said semiconductor wafer and in which the four peripheral sides form a semiconductor chip which has { 110 } sides.

[Claim 9] In [are a manufacturing method of a semiconductor memory device characterized by comprising the following, and] said plane direction setting process, Set a main table side of said semiconductor wafer as { 100 } sides, and an orientation flat is set as { 110 } sides, [an active region which intersects perpendicularly with a gate electrode which constitutes said MOS type field effect transistor in said circuit element pattern process, and a longitudinal direction of this gate electrode, and extends] It is patterned so that it may intersect [it is parallel or] perpendicularly and extend in the direction of dicing of said dicing process, And in [said slot type capacitor is patterned so that it may become the square pole form which has a horizontal section of a rectangle which makes an angle of 45 degrees in said direction of dicing, and] said dicing process, A manufacturing method of a semiconductor device by which dicing is carried out in a direction and a parallel direction which intersect perpendicularly with said orientation flat so that four peripheral sides of said semiconductor chip may turn into { 110 } sides.

A plane direction setting process of setting a semiconductor wafer as a predetermined plane direction.

A circuit element pattern process which patterns a circuit element which contains in said semiconductor wafer a memory cell which has a MOS type field effect transistor and slot type capacitor, and a dicing process which cuts said semiconductor wafer to a semiconductor chip of a rectangular parallelepiped.

[Detailed Description of the Invention]

[0001]

[Industrial Application] Especially this invention relates to structure of the slot type capacitor formed on a semiconductor chip, and a manufacturing method for the same about a semiconductor device and a manufacturing method for the same.

[0002]

[Description of the Prior Art] In recent years, the demand has expanded the semiconductor device quickly by the remarkable spread of information machines and equipment, such as a computer. It has a large-scale storage capacity functionally, and the thing which can be worked high-speed is demanded. Under such a background, engineering development about high integration and high speed response nature, or high-reliability is furthered in the semiconductor device.

[0003] DRAM (Dynamic Random Access Memory) is one of those in which the random input/output of memory information is possible among semiconductor devices. Generally

DRAM comprises a memory cell array which is a storage area which accumulates much memory information, and a peripheral circuit required for an input/output with the exterior.

[0004]Drawing 36 is a block diagram showing the composition of general DRAM. DRAM50 with reference to drawing 36 The memory cell array 51 and the low and column address buffer 52, The row decoder 53 and the column decoder 54, the sense refreshment amplifier 55, the data in buffer 56 and the data out buffer 57, and the clock generator 58 are included.

[0005]The memory cell array 51 is for accumulating the data signal of memory information. The low and column address buffer 52 is for receiving address signal A_0 for choosing the memory cell which constitutes a unit memory circuit - A_9 from the exterior. The row decoder 53 and the column decoder 54 are for specifying a memory cell by decoding the address signal. The sense refreshment amplifier 55 is for amplifying and reading the signal accumulated in the specified memory cell. The data in buffer 56 and the data out buffer 57 are the things for a data input/output. The clock generator 58 generates the clock signal used as the control signal to each part.

[0006]Two or more memory cells for accumulating unit memory information are arranged by matrix form, and the memory cell array 51 which occupies a big area on a semiconductor chip is formed. Drawing 37 is a figure showing the equal circuit for 4 bits of the memory cell which constitutes the memory cell array 51. The memory cell array 51 is provided with the two or more word line WL prolonged in parallel with a line writing direction, and two or more bit line pairs BLaBLb prolonged in parallel with a column direction. The memory cell M is formed near the intersection of the word line WL and the bit line BLaBLb.

[0007]The memory cell M consists of the one MOS (Metal Oxide Semiconductor) model field-effect transistor Tr and the one capacitor C. That is, each memory cell shows the what is called 1 transistor 1 capacitor type memory cell. In order to attain high integration, the slot type capacitor with which the slot was formed in the depth direction of a substrate is used for this capacitor C. Since this type of memory cell is simple for that structure, it is easy to raise the degree of location of a memory cell array, and is widely used for mass DRAM.

[0008]Two or more DRAMs mentioned above on the other hand are formed on the semiconductor chip.

This semiconductor chip is formed of what a semiconductor wafer is cut down for in predetermined shape (dicing).

[0009]Conventionally, after patterning DRAM etc. after a semiconductor wafer using vapor deposition art, oxidization art, phototype process art, etc., dicing of the semiconductor wafer is carried out and a semiconductor chip is completed.

[0010]When using phototype process art etc. for a semiconductor wafer and forming DRAM in it, patterning is performed on the basis of the orientation flat by which the patterning was generally provided in the semiconductor wafer. Usually, the plane direction of the main table side of a semiconductor wafer is set as {100} sides, and DRAM will be formed in this main table side. As for the orientation flat, the thing of {110} sides and {100} sides exists and the plane direction is properly used in the use.

[0011]The structure of a slot type capacitor where the main table side of a semiconductor wafer is hereafter formed in respect of {100} in DRAM in case an orientation flat is

{100} sides or {110} sides is explained below.

[0012]First, the case where the main table sides of a semiconductor wafer are {100} sides, and orientation flats are {110} sides is explained.

[0013]With reference to drawing 38, {100} sides are formed for the main table side 61a, and semiconductor devices, such as DRAM, are already formed in the semiconductor wafer 60 of {110} sides for the orientation flat 61b. Two or more dicing lines 62 and 63 are formed in this semiconductor wafer 60 perpendicularly or in parallel to the orientation flat 61b. Two or more semiconductor chips 64 are formed by carrying out dicing of the semiconductor wafer 60 along with these dicing lines 62 and 63.

[0014]Next, as for {100} sides and the four peripheral sides 64b, 64c, 64d, and 64e, in the plane direction of the semiconductor chip 64 which is one of the plurality formed by the above, with reference to drawing 39, the main table side 64a is set as {110} sides. Two or more memory cells 65 which constitute the memory cell array formed in DRAM are formed in the main table side 64a.

[0015]Next, the structure of the memory cell 65 is explained with reference to drawing 40 and drawing 41.

[0016]Drawing 40 is a top view of the memory cell 65. Drawing 41 is a X-X line arrowed cross-section figure in drawing 40.

[0017]The memory cell 65 comprises MOS type field effect transistor 66 and the slot type capacitor 67. MOS type field effect transistor 66 is formed in the intersection of the active region 66b which intersects perpendicularly with the longitudinal direction of the gate electrode 66a which consists of word lines, and this gate electrode 66a abbreviated, and extends. The slot type capacitor 67 is formed in the active region 66b. The bit line 66c is wired in the upper part of the active region 66b. The contact hole 66e for connection with this bit line 66c and substrate is formed.

[0018]Here, patterning for the element formation to the semiconductor wafer 60 is patterned so that arrangement of each element may usually become in parallel or perpendicular on the basis of an orientation flat. This is determined in consideration of improvement in the integration density of each element formed in a semiconductor wafer, the error at the time of patterning, and the workability at the time of dicing. Therefore, with reference to drawing 42, the 4-round insides 67a, 67b, 67c, and 67d of the slot type capacitor 67 formed in the semiconductor chip 64 turn into {110} sides, and the bottom 67e turns into {100} sides.

[0019]However, when forming an oxidizing film by thermal oxidation on a semiconductor surface, it is known in respect of {100} and {110} that oxidization speed differs. For example, when {110} sides are oxidized on the same conditions as forming a 100-A oxide film in respect of {100}, a 150-A oxide film is formed and it turns out that the direction of {100} sides has a slow oxidization speed. This shows that it is [control of oxide film formation] easier to form an oxide film in {100} sides. Having problems, like crystal density has more {110} sides and control of threshold voltage is more difficult than {100} sides is known. Therefore, as for the plane direction of the 4-round inside of the slot type capacitor 67, and a plane direction at the bottom, it is desirable that they are {100} sides.

[0020]Then, a main table side explains below the case where {100} sides and an orientation flat form DRAM on the semiconductor wafer 70 of {100} sides, with reference to the contents indicated by JP,S60-253263,A, for example.

[0021]With reference to drawing 43, {100} sides are formed for the main table side 71a, and DRAM is already formed for the orientation flat 71b on the semiconductor wafer 70 of {100} sides. Two or more dicing lines 72 and 73 are formed in this semiconductor wafer 70 perpendicularly or in parallel at the orientation flat 71b.

[0022]Next, as for {100} sides and the four peripheral sides 74b, 74c, 74d, and 74e, in the plane direction of the semiconductor chip 74 cut along with the above-mentioned dicing lines 72 and 73, with reference to drawing 44, the main table side 74a is set as {100} sides. DRAM currently formed on the main table side 74a is formed like the semiconductor chip 64 mentioned above. Therefore with reference to drawing 45, the 4-round insides 80a, 80b, 80c, and 80d of the slot type capacitor 80 formed in the memory cell 65 are set as {100} sides, and the bottom 80e is set as {100} sides, and can make {100} sides all the inside of a slot sides.

[0023]By this, the oxide film thicknesses formed in the slot type capacitor 80 can be formed equally, and improvement in the reliability of a memory cell can be aimed at.

[0024]

[Problem to be solved by the invention]However, when the above-mentioned semiconductor wafer 70 is used and the semiconductor chip 74 is cut down by dicing, a semiconductor chip has a problem of being easy to produce a crack.

[0025]Here, the characteristics of a crack of a silicon wafer are explained with reference to drawing 46 thru/or drawing 48.

[0026]The physical relationship of the plane direction of a silicon wafer can be denoted by the model of 26 face pieces with reference to drawing 46. in the plane direction of {111} sides, as characteristics of a crystal face, a defect and stress occur most -- ***** - - things are already known. For example, the characteristics of a crack [the main table side 71a / {100} sides and the orientation flat 71b] of the silicon wafer 70 of {100} sides break in the 45-degree direction easily to the cross line of an orientation flat and a main table side with reference to drawing 47 and drawing 48. This is because the cross line of the {111} sides of the silicon wafer 70 of {100} sides and the main table side 71a makes the angle of 45 degrees to the orientation flat 71b and the main table side 71a and the orientation flat 71b exist.

[0027]Thus, when the cross line of the {111} sides of a silicon wafer whose main table sides are {100} sides and whose orientation flats are {100} sides, and a main table side makes the angle of 45 degrees and exists to an orientation flat, The direction of dicing for forming a semiconductor chip from a silicon wafer is perpendicular or parallel to an orientation flat. Therefore, it becomes easy to produce a crack in the diagonal direction of a semiconductor chip at the time of dicing of a semiconductor wafer. moreover -- stress, such as heat treatment in a manufacturing process, makes the diagonal direction of a semiconductor chip generate a crack, and produces a remarkable problem in the fall of the yield of a chip, and the reliability of a function -- ** -- now, it is.

[0028]On the other hand, since the cross line of the main table side 61a and {111} sides exists perpendicularly or in parallel to an orientation flat when the semiconductor wafer 60 of conventional technology is used, are solving the above-mentioned problem, but. The problem that the oxide film in a slot type capacitor is uneven is unsolvable.

[0029]While this invention was made in order to cancel the above-mentioned problem, and it can form equally the oxide film thicknesses formed in a slot type capacitor portion and maintaining facilitating of element design manufacture of a slot type capacitor, The

crack to that of the semiconductor chip at the time of dicing cannot enter easily, and providing a semiconductor device with high reliability which does not go into a chip diagonal direction, and a manufacturing method for the same has a crack by the stress in process treatment, such as heat treatment.

[0030]

[Means for solving problem]The semiconductor device according to this invention is provided with the following.

{100} sides and four peripheral sides are provided with the semiconductor substrate which has {110} sides in one aspect of affairs, and a main table side, [the cross line of the {111} sides of this semiconductor substrate, and the above-mentioned main table side] The 1st conductive layer it existed in the four above-mentioned peripheral side in parallel or perpendicularly, and the slot where the inside was set as {100} sides 4 round was formed in the main table side of the above-mentioned semiconductor substrate, and was formed over at least one inside of this slot.

The insulating layer formed on at least one inside of this 1st conductive layer.

The 2nd conductive layer formed in the upper surface of this insulating layer.

[0031]The semiconductor device according to this invention is provided with the following.

The semiconductor substrate which has a main table side and four peripheral sides in other aspects of affairs.

The MOS type field effect transistor and slot type capacitor which were formed on the main table side of this semiconductor substrate.

In the main table side of the above-mentioned semiconductor substrate, {100} sides and four peripheral sides are set as {110} sides. The above-mentioned slot type capacitor is formed in the slot on the square pole form where an inside consists of {100} sides the 4 round.

[0032]The semiconductor device according to this invention is provided with the following.

The semiconductor chip of the 1st conductivity type that makes a rectangular parallelepiped in other aspects of affairs.

The MOS type field effect transistor and slot type capacitor which were formed on the main table side of this semiconductor chip.

In the main table side of the above-mentioned semiconductor chip, {100} sides and four peripheral sides are formed from {110} sides. The above-mentioned MOS type field effect transistor includes the active region which extends in the direction which intersects perpendicularly with the gate electrode prolonged in parallel or the right-angled direction, and this gate electrode in four peripheral sides of the above-mentioned semiconductor chip. The above-mentioned slot type capacitor is formed in the slot on the square pole form where the four peripheral sides consist of {100} sides.

[0033]The semiconductor device according to this invention is a semiconductor chip in which {100} sides and four peripheral sides have {110} sides in a main table side in the aspect of affairs of further others. The slot type capacitor is formed on this semiconductor chip. This slot type capacitor has the slot where the inside was set as {100} sides 4 round, and the cross line of the {111} sides of the above-mentioned semiconductor chip and the above-mentioned main table side exists in the main table side of the above-mentioned

semiconductor chip in parallel or perpendicularly.

[0034][the semiconductor device according to this invention] [the aspect of affairs of further others] The semiconductor substrate which has a slot which is formed in the depth direction of a substrate from a main table side, four peripheral sides, and a main table side, and has an inside 4 round, It has the MOS field-effect transistor which has one pair of impurity ranges formed so that the field of the semiconductor substrate in alignment with the inside of the above-mentioned slot might be made into channel regions, the gate dielectric film formed on the above-mentioned channel regions, and the gate electrode which is on the above-mentioned gate dielectric film, and was formed in the inside of the above-mentioned slot. As for {100} sides and four peripheral sides, {110} sides and the above-mentioned 4-round inside are formed for the above-mentioned main table side from {100} sides.

[0035]As for the manufacturing method of the semiconductor device according to this invention, the slot where the inside was set to the semiconductor wafer in which a main table side has {110} sides first in one aspect of affairs that 4 round in {100} sides is formed. The 1st conductive layer is formed over at least one inside of this slot. An insulating layer is formed on at least one inside of this 1st conductive layer. The 2nd conductive layer is formed in the upper surface of this insulating layer. Dicing of the above-mentioned semiconductor wafer is carried out along the direction of the cross line of the above-mentioned main table side and the {111} sides of the above-mentioned semiconductor wafer, and the semiconductor chip in which the four peripheral sides have {110} is formed.

[0036]The manufacturing method of the semiconductor device according to this invention, [other aspects of affairs] The semiconductor wafer of the 1st conductivity type was set as the predetermined plane direction, the memory device which has an MOS field-effect transistor and a slot type capacitor in a semiconductor wafer was formed, and it has the process of carrying out dicing of the above-mentioned semiconductor wafer to the semiconductor chip which has a main table side and four peripheral sides. The slot where the inside was set as {100} sides the 4 round is formed in the main table side of the above-mentioned semiconductor wafer. An MOS field-effect transistor is formed in the main table side of the above-mentioned semiconductor wafer. A capacitor is formed over at least one inside of the above-mentioned slot. Dicing of the above-mentioned semiconductor wafer is carried out along the direction of the cross line of the {111} sides of the above-mentioned semiconductor wafer, and the above-mentioned main table side. Four peripheral sides of the above-mentioned semiconductor wafer are formed in the semiconductor chip which has {110} sides.

[0037][the manufacturing method of the semiconductor device according to this invention] [the aspect of affairs of further others] First, it is the method of manufacturing the semiconductor device provided with the MOS field-effect transistor on the semiconductor wafer which has a main table side of {100} sides, and the slot where the inside was set as {100} sides the 4 round is formed in the main table side of the above-mentioned semiconductor wafer. The ion implantation of the impurities is carried out to the inside of this slot, and a source/drain area is formed. Gate dielectric film is formed of thermal oxidation on the inside of the above-mentioned slot. A gate electrode is formed on the above-mentioned gate dielectric film by the above-mentioned inside of a slot. Dicing of the above-mentioned semiconductor wafer is carried out in the direction of

the cross line of the {111} sides of the above-mentioned semiconductor wafer. The four above-mentioned peripheral side is formed in the semiconductor chip which has {110} sides.

[0038][the manufacturing method of the semiconductor device according to this invention] [the aspect of affairs of further others] Set a semiconductor wafer as a predetermined plane direction, and the circuit element containing the memory cell which has a MOS type field effect transistor and slot type capacitor in this semiconductor wafer is patterned, It is a manufacturing method of the semiconductor device provided with the process of cutting the above-mentioned semiconductor wafer to the semiconductor chip of a rectangular parallelepiped, and the main table side of the above-mentioned semiconductor wafer is set as {100} sides. An orientation flat is set as {110} sides. The active region which intersects perpendicularly with the gate electrode which constitutes the above-mentioned MOS type field effect transistor, and the longitudinal direction of this gate electrode, and extends is patterned so that it may intersect [it is parallel or] perpendicularly and extend in the above-mentioned dicing direction. It is patterned so that each neighborhood of the above-mentioned slot type capacitor may become the square pole form which has a horizontal section of the rectangle which makes the angle of 45 degrees in the above-mentioned dicing direction. Dicing is carried out in the direction perpendicular to the above-mentioned orientation flat, and parallel so that all of four peripheral sides of the above-mentioned semiconductor chip may become {110} sides.

[0039]

[Function]In the main table side of a semiconductor chip, {100} sides and four peripheral sides consist of {110} sides in this invention. The slot which has an inside 4 round is patterned after the square pole form which has a horizontal section of the rectangle which makes the angle of 45 degrees in the direction of dicing. Thereby, as for the slot formed on this semiconductor chip, an inside is set as {100} sides that 4 round. The semiconductor wafer whose main table sides are {100} sides and whose orientation flats are {110} sides is used, When dicing is carried out in the direction perpendicular to an orientation flat, or parallel, the cross line of the {111} sides on a semiconductor and the main table side of a semiconductor wafer becomes a relation parallel to the direction of dicing, or perpendicular.

[0040][by maintaining the direction of dicing in the direction and the parallel direction which intersect perpendicularly with an orientation flat side, and making the plane direction of the 4 round inside of a slot into {100} sides] To an orientation flat, lean the fall of the degree of location of the circuit element by leaning 45 degrees of all the circuit elements to an orientation flat, and 45 degrees of the whole semiconductor chip, and they are formed, Aggravation of the workability at the time of leaning 45 degrees of dicing lines to an orientation flat, etc. can be prevented.

[0041]

[Working example]Hereafter, one embodiment at the time of applying to especially DRAM is described with reference to drawing 1 thru/or drawing 9 about the embodiment of a semiconductor device based on this invention.

[0042]First, with reference to drawing 1, the memory cell 5 is formed on the semiconductor chip 3 of the rectangular parallelepiped which consists of single crystals. In drawing 1, two or more memory cells 5 are formed in practice, although only one

piece is written for convenience.

[0043]Next, the structure of the memory cell 5 is explained with reference to drawing 2 and drawing 3. Drawing 2 is a top view of the memory cell 5. Drawing 3 is a X-X line arrowed cross-section figure in drawing 2.

[0044]On the main table side of a semiconductor chip, the gate electrode 6a which is parallel to the four peripheral sides 3b, 3c, 3d, and 3e of the semiconductor chip 3, or is prolonged perpendicularly is formed. The active region 6b is formed in the direction which intersects perpendicularly with this gate electrode 6a. The bit line 6c is wired by the upper surface of this active region 6b.

[0045]The source region 13 and the drain area 14 which consist of n type impurities are formed in the active region 6b of a gate electrode 6a directly under which intersects this bit line 6c. MOS type field effect transistor 6 is formed of the above-mentioned gate electrode 6a, the oxide film 7g and the source region 13, and the drain area 14. The slot 7a on the square pole form is formed in the active region 6b. The 4-round inside of this slot 7a is making four peripheral sides of the semiconductor chip 3, and 45-degree inclination. 7 f of conductive layers which consist of n type impurities of a prescribed depth are formed from the inside of this slot 7a. The oxide film 7g is formed in the upper surface of 7 f of this conductive layer. The inside of the slot 7a is filled up with the polycrystalline silicon 7h via this oxide film 7g. The slot type capacitor 7 is formed with 7 f of the above-mentioned conductive layers, the oxide film 7g, and the polycrystalline silicon 7h. 7 f of conductive layers are electrically connected with the above-mentioned drain area 14. Thereby, above-mentioned MOS type field effect transistor 6 and the above-mentioned slot type capacitor 7 constitute a what is called 1 transistor 1 capacitor type memory cell. On the main table side of the semiconductor substrate 4, the contact hole 9 for connection between the bit line 6c and a substrate is also formed.

[0046]Here, dicing of the silicon wafer 1 is carried out, and the semiconductor chip 3 in which two or more above-mentioned memory cells 5 were formed is formed, as shown in drawing 4. In the plane direction of the above-mentioned silicon wafer 1, in this example, {100} sides and the orientation flat 1b consist [the main table side 1a] of {110} sides. In the direction of dicing of the silicon wafer 1, dicing is performed by the parallel line 2a and the perpendicular line 2b to the orientation flat 1b. Thereby, with reference to drawing 5, the four peripheral sides 3a, 3b, 3c, and 3d of the semiconductor chip 3 serve as a plane direction of {110} sides altogether. With reference to drawing 6, all the plane directions of the 4-round insides 7a, 7b, 7c, and 7d of the slot formed in the memory cell 5 and the bottom 7e will be set as {100} sides, and it becomes possible to form equally the film thickness of the oxide film of all the fields.

[0047]On the other hand, the characteristics of a crack of the above-mentioned silicon wafer are explained with reference to drawing 7 thru/or drawing 9. The physical relationship of the plane direction of the silicon wafer 1 can be denoted by the model of 26 face pieces, as shown in drawing 7. As characteristics of a crystal face, {111} plane directions are already known that it is the easiest to generate a defect and stress. The main table side 1a breaks in the parallel or perpendicular direction easily to the orientation flat 1b, as {100} sides and the orientation flat 1b show drawing 8 and drawing 9 the characteristics of a crack of the silicon wafer 1 of {110} sides. The main table sides 1a are {100} sides, and the orientation flat 1b of this is because the cross line 11 of the {111} sides of the silicon wafer 1 of {110} sides and the main table side 1a becomes

parallel or perpendicular physical relationship to the orientation flat 1b. Therefore, when dicing separates the silicon wafer 1 into a semiconductor chip, the cross line of a dicing line, {111} sides, and a main table side serves as parallel physical relationship.

[0048]By the above, formation of the film thickness of an oxide film can be made uniform by making the 4-round inside and the bottom of a slot into a main table side and the same {100} sides. Since the cross line of a dicing line, {111} sides, and a main table side becomes parallel, it becomes possible to prevent a chip of the tip end part at the time of dicing.

[0049]Next, the manufacturing method of the memory cell 5 which consists of the above-mentioned structure is explained with reference to drawing 10 thru/or drawing 18.

[0050]With reference to drawing 11, the main table side 1a of the silicon wafer (henceforth a substrate) 1 in which the memory cell 5 is formed is first set as {100} sides, and the orientation flat 1b is set as {110} sides. Then, LOCOS process is used for the substrate 1 and the field oxide 8 is formed by selective oxidation.

[0051]Next, the resist layer 10 is applied to a substrate face with reference to drawing 12, and a resist layer is patterned with phototype process art using the reticle mask 30 which has the square hole to which 45 degrees inclined to the orientation flat datum level shown in drawing 10. Then, the slot 72 on the square pole form to which 45 degrees of 4-round insides of the slot inclined to the orientation flat side by anisotropic etching is formed. By this, the plane direction of the 4-round insides 72a, 72b, 72c, and 72d of the slot 72 and the bottom 72e will be set as {100} sides.

[0052]Next, with reference to drawing 13, it leaves only the portion pinched by the slot 72 of the above-mentioned resist layer 10, and other resist layers 10 are removed. Then, boron etc. are injected into the substrate 1 by slanting rotation ion implantation, and 7 f of n type conductive layers are formed in a substrate face, 4 rounds of slot inside, and the bottom.

[0053]Next, with reference to drawing 14, about 50-100Å of oxide films 7g which become the main table side 1a of the substrate 1, and the 4-round insides 72a, 72b, 72c, and 72d and the groove bottom side 72e of the slot 72 from SiO₂ by a thermal oxidation method are formed in the whole surface. At this time, since the plane direction of the main table side 1a, the 4-round insides 72a, 72b, 72c, and 72d of the slot 72, and the bottom 72e is altogether set as {100} sides as mentioned above, it can form a uniform oxide film altogether.

[0054]Next, with reference to drawing 15, the polysilicon 7h is deposited all over the inside of the slot 72, and a substrate face. Then, in order to remove the polysilicon 7h deposited on the field in which a MOS type field effect transistor is formed with reference to drawing 16, the resist layer 12 which has predetermined shape and to carry out is formed, and anisotropic etching removes the polysilicon 7h.

[0055]Next, after forming the gate electrode 6a with reference to drawing 17, n type impurities, such as boron, are poured in substrate 1, and the source region 13 and the drain area 14 which consist of a n type impurity diffusion region are formed. At this time, the drain area 14 is electrically connected with the conductive layer 75.

[0056]Next, with reference to drawing 18, the interlayer insulation film 15 which consists of SiO₂ etc. is formed in the substrate 1 surface. After forming in the interlayer insulation film 15 the contact hole 9 which passes to the account source region 13 of Gokami, the bit line 6c which becomes the substrate 1 surface from a polycide is formed in the

direction which intersects perpendicularly in the direction in which the gate electrode 6a is prolonged. The semiconductor device in this example is completed by the above.

[0057]In the above-mentioned embodiment, although single crystal silicon was used for the semiconductor wafer, even if it uses the silicon formed by epitaxial growth, the same effect is acquired, without being restricted to this. The same effect is acquired also in the compound semiconductor containing gallium arsenide (GaAs), an indium phosphorus (InP), silicon germanium (germanium/Si), etc.

[0058]On the other hand, even if the composite membrane which consists of an oxide film and a nitride is used for the oxide film 7g formed in slot type capacitor 7 inside, it can acquire the same effect.

[0059]In the above-mentioned embodiment, although 7f of n type conductive layers are provided as a lower electrode of a capacitor, as shown in drawing 19, by using a p type semiconductor substrate, the n type semiconductor device 7f can be made unnecessary, and it can be considered as the lower electrode of a capacitor using this p type semiconductor substrate.

[0060]Next, other embodiments of the DRAM memory cell according to this invention are described. With reference to drawing 20, two or more memory cells 17 are formed [the main table side where the main table side started according to {100} sides, and the orientation flat cut down the P type silicon wafer of {110} sides by dicing] in the main table side 16a of the semiconductor chip 16 of {110} sides for {100} sides and four peripheral sides.

[0061]Drawing 21 is a top view of the memory cell 17. Drawing 22 is a Y-Y line arrowed cross-section figure in drawing 21.

[0062]With reference to drawing 21, two or more bit lines 19 which consist of an n⁺ impurity range are formed in the direction parallel to the four peripheral sides, or perpendicular on the p type semiconductor substrate 21. Two or more word lines 18 are formed in the perpendicular direction to this bit line 19. The slot 20 where the inside made the angle of 45 degrees to the above-mentioned bit line or the word line direction on the intersection of the above-mentioned bit line 19 and the word line 18 4 round is formed.

[0063]Next, with reference to drawing 22, the memory cell 17 by which isolation was carried out with the isolation oxide film 25 on the main table side of the p type semiconductor substrate 21 is formed. This memory cell 17 comprises an n channel MOS type field-effect transistor and a slot type capacitor.

[0064]The n channel MOS type field-effect transistor has the n⁺ impurity ranges 19 and 26 which constitute a drain/source region, the channel regions 105 provided among them, and the gate electrode 18 which made the gate oxide 24 intervene and was formed on the channel regions 105. These channel regions 105 exist in the lower part of the gate oxide 24 in alignment with the side wall part of the slot formed on the main table side of the p type semiconductor substrate 21.

[0065]A capacitor consists of the capacitor electrode 23 formed so that it might connect with the n⁺ impurity range 26 which constitutes an n channel MOS type field-effect transistor, the capacitor oxide film 22, and the p type semiconductor substrate 21.

[0066]This capacitor electrode 23 consists of a polysilicon layer embedded in the trench formed in the p type silicon substrate 21. The n⁺ impurity range 26 is formed on the circumference of the capacitor electrode 23 at all the circumferences. The gate electrode

18 which constitutes an n channel MOS type field-effect transistor consisted of an n⁺ polysilicon layer, and serves as the word line. Thereby, the n channel MOS type field-effect transistor of the method of length is formed in the side wall part of the slot established in capacitors.

[0067]Next, the manufacturing method of the memory cell of DRAM according to this embodiment is explained. Drawing 23 - drawing 34 are the sectional views showing the manufacturing method of the memory cell of this invention at process order according to the section structure shown in drawing 22.

[0068]With reference to drawing 23, LOCOS process is used for the main table side of the p type semiconductor substrate 21, and the isolation oxide film 25 is formed in it. Next, the resist layer 27 is applied to the surface of the substrate 21 with reference to drawing 24. Then, a resist layer is patterned with phototype process art using the reticle mask (refer to drawing 10) which has two or more square holes to which 45 degrees inclined to the orientation flat datum level and to carry out. The side of a slot forms after that the slot 20 on the square pole form to which 45 degrees inclined to the orientation flat side by anisotropic etching. Thereby, the plane direction of the 4-round inside of a slot and the bottom is set as {100} sides.

[0069]Next, with reference to drawing 25, the about 50-100-Å-thick oxide film 22 is formed by a thermal oxidation method all over the inside of the slot 20, and a substrate face. At this time, since the 4-round inside and the bottom of the slot are set as {100} sides, they can form a uniform oxide film.

[0070]Next, drawing 26 is referred to and it is a wrap about the resist 28 to the inside and the whole main table side surface of the slot 20. Next, with reference to drawing 27, only the predetermined depth leaves the resist 28 for the above-mentioned resist layer 28 in the slot 20 by the etchback method.

[0071]Next, with reference to drawing 28, the oxide film 22 is alternatively removed by using as a mask the resist 28 left behind in the slot 20, and the oxide film 22 used as the capacitor insulating film of a capacitor is formed in the bottom of the slot 20.

[0072]Next, with reference to drawing 29, the n⁺ polysilicon 23 is deposited all over an inside of a slot part and a substrate face. Next, with reference to drawing 30, a resist layer (not shown) is applied to the upper surface of the n⁺ polysilicon 23, and by the etchback method, etchback of the n⁺ polysilicon 23 is carried out, and it leaves the n⁺ polysilicon 23 by predetermined Mr. Fukashi in the slot 20. This polysilicon 23 serves as a capacitor electrode of a capacitor.

[0073]Next, with reference to drawing 31, by performing annealing treatment to the above-mentioned n⁺ polysilicon 23, the impurities in the n⁺ polysilicon layer 23 are spread inside the silicon substrate 21, and the n⁺ impurity range 26 is formed.

[0074]Next, the n⁺ impurity range 19 used as a bit line is formed by carrying out the ion implantation of the n type impurities, such as a phosphorus (P), to a substrate face, and carrying out thermal diffusion to it with reference to drawing 32.

[0075]Next, with reference to drawing 33, the gate dielectric film 24 is formed with CVD all over the n⁺ polysilicon 23 of an inside of a slot part, the 4-round inside of a slot, and a substrate face. Also at this time, since the 4-round inside and substrate face of the slot are set as {100} sides, a uniform oxide film can be formed.

[0076]Next, with reference to drawing 34, the word line 18 which consists of polysilicon etc. is formed in an inside of a slot part and a substrate face. By the above, the memory

cell of DRAM according to this invention is completed.

[0077]It becomes possible to make uniform formation of the oxide film of a main table side and an inside of a slot side by making into {100} sides the plane direction of the 4-round inside of the slot established in the substrate as mentioned above. It becomes possible to form a MOS type field effect transistor in the slot side, and it becomes possible to attain the miniaturization of a memory cell, and the densification of DRAM.

[0078]Next, the embodiment of further others of the DRAM memory cell according to this invention is described.

[0079]With reference to drawing 35, as compared with the embodiment of DRAM explained previously, the channel regions 105 which constitute an n channel MOS type field-effect transistor apply DRAM in this embodiment to the side wall of a slot from a substrate face, and it is formed.

[0080]Thus, even if it forms an n channel MOS type field-effect transistor so that an inside of a slot side may be straddled from a substrate face since a substrate face is set as {100} sides and the inside of a slot side is set as {100} sides, the same operation effect as the above can be obtained.

[0081]

[Effect of the Invention]As mentioned above, according to this invention, a main table side uses the silicon wafer which has {100} sides and an orientation flat {110} side, [four peripheral sides of a semiconductor chip] [{110} sides and the 4 round inside of the slot type capacitor formed in a semiconductor chip] [considering it as {100} sides] The oxide film thicknesses formed each neighborhood of a slot type capacitor can be formed equally, facilitating of the design manufacture of the element of a slot type capacitor is carried out, and it makes it possible to attain equalization stabilization of an element characteristic.

[0082]Since the cross line of a dicing line, the {111} sides of a silicon wafer, and a main table side serves as parallel physical relationship when dicing separates a silicon wafer into a semiconductor chip, It makes it possible to prevent a chip of the tip end part at the time of dicing, and to prevent beforehand the crack initiation to the chip by the stress at the time of process treatment, such as heat treatment. The cost cut of a semiconductor chip is invited and the above enables it to aim at improvement in the reliability of the function of a semiconductor device.

[Brief Description of the Drawings]

[Drawing 1]It is a figure showing superficial arrangement of the memory cell according to this invention.

[Drawing 2]It is a part plan showing the superficial arrangement of a memory cell based on this invention.

[Drawing 3]It is a section structural drawing in the X-X line in drawing 1.

[Drawing 4]It is a perspective view of a silicon wafer according to this invention.

[Drawing 5]It is a figure showing the relation of the plane direction of four peripheral sides of the semiconductor chip according to this invention.

[Drawing 6]It is a figure showing the relation of the plane direction of the 4-round inside of a slot type capacitor based on this invention.

[Drawing 7]It is a figure of a model showing the relation of the plane direction of the silicon wafer according to this invention.

[Drawing 8]It is a figure showing the characteristics of the crack of a silicon wafer according to this invention.

[Drawing 9]It is a figure showing the state of the crack of a silicon wafer according to this invention.

[Drawing 10]It is a detail view of the reticle mask according to this invention.

[Drawing 11]It is a sectional view showing the 1st process of the 1st embodiment of the manufacturing method of the memory cell according to this invention.

[Drawing 12]It is a sectional view showing the 2nd process of the 1st embodiment of the manufacturing method of the memory cell according to this invention.

[Drawing 13]It is a sectional view showing the 3rd process of the 1st embodiment of the manufacturing method of the memory cell according to this invention.

[Drawing 14]It is a sectional view showing the 4th process of the 1st embodiment of the manufacturing method of the memory cell according to this invention.

[Drawing 15]It is a sectional view showing the 5th process of the 1st embodiment of the manufacturing method of the memory cell according to this invention.

[Drawing 16]It is a sectional view showing the 6th process of the 1st embodiment of the manufacturing method of the memory cell according to this invention.

[Drawing 17]It is a sectional view showing the 7th process of the 1st embodiment of the manufacturing method of the memory cell according to this invention.

[Drawing 18]It is a sectional view showing the 8th process of the 1st embodiment of the manufacturing method of the memory cell according to this invention.

[Drawing 19]It is a section structural drawing in other embodiments of the memory cell which is different in this invention.

[Drawing 20]It is a top view showing the superficial arrangement in other embodiments of the memory cell according to this invention.

[Drawing 21]It is a part plan showing the superficial arrangement in other embodiments of the memory cell according to this invention.

[Drawing 22]It is a Y-Y line arrowed cross-section figure in drawing 21.

[Drawing 23]It is a sectional view showing the 1st process in other embodiments of the manufacturing method of the memory cell according to this invention.

[Drawing 24]It is a sectional view showing the 2nd process in other embodiments of the manufacturing method of the memory cell according to this invention.

[Drawing 25]It is a sectional view showing the 3rd process in other embodiments of the manufacturing method of the memory cell according to this invention.

[Drawing 26]It is a sectional view showing the 4th process in other embodiments of the manufacturing method of the memory cell according to this invention.

[Drawing 27]It is a sectional view showing the 5th process in other embodiments of the manufacturing method of the memory cell according to this invention.

[Drawing 28]It is a sectional view showing the 6th process in other embodiments of the manufacturing method of the memory cell according to this invention.

[Drawing 29]It is a sectional view showing the 7th process in other embodiments of the manufacturing method of the memory cell according to this invention.

[Drawing 30]It is a sectional view showing the 8th process in other embodiments of the manufacturing method of the memory cell according to this invention.

[Drawing 31] It is a sectional view showing the 9th process in other embodiments of the manufacturing method of the memory cell according to this invention.

[Drawing 32] It is a sectional view showing the 10th process in other embodiments of the manufacturing method of the memory cell according to this invention.

[Drawing 33] It is a sectional view showing the 11th process in other embodiments of the manufacturing method of the memory cell according to this invention.

[Drawing 34] It is a sectional view showing the 12th process in other embodiments of the manufacturing method of the memory cell according to this invention.

[Drawing 35] It is a section structural drawing in the embodiment of further others of the memory cell according to this invention.

[Drawing 36] It is a block diagram showing the entire configuration of the conventional dynamic random access memory (DRAM).

[Drawing 37] It is a representative circuit schematic showing the sense amplifier of DRAM and the memory cell for 4 bits of a memory cell array which were shown in drawing 36.

[Drawing 38] It is the whole silicon wafer perspective view based on conventional technology.

[Drawing 39] It is a top view showing superficial arrangement of the memory cell according to conventional technology.

[Drawing 40] It is a part plan showing superficial arrangement of the memory cell according to conventional technology.

[Drawing 41] It is a X-X arrowed cross-section figure in drawing 40.

[Drawing 42] It is a figure showing arrangement of the slot type capacitor in conventional technology.

[Drawing 43] It is the whole semiconductor wafer perspective view based on conventional technology.

[Drawing 44] It is a top view showing superficial arrangement of the memory cell according to conventional technology.

[Drawing 45] It is a part plan showing superficial arrangement of the memory cell according to conventional technology.

[Drawing 46] It is a figure of a model showing the relation of the plane direction of the silicon wafer in conventional technology.

[Drawing 47] It is a figure showing the characteristics of a crack of the silicon wafer in conventional technology.

[Drawing 48] It is a figure showing the state of a crack of the silicon wafer in conventional technology.

[Explanations of letters or numerals]

1, 16 semiconductor wafers

1a Main table side

1b Orientation flat

2a and 2b Dicing line

3, 16 semiconductor chips

5 and 17 Memory cell

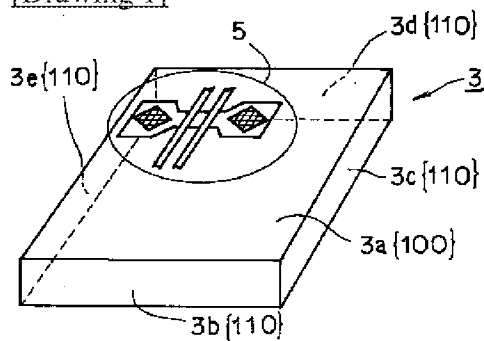
6 Field-effect transistor

6a, 18 gate electrodes

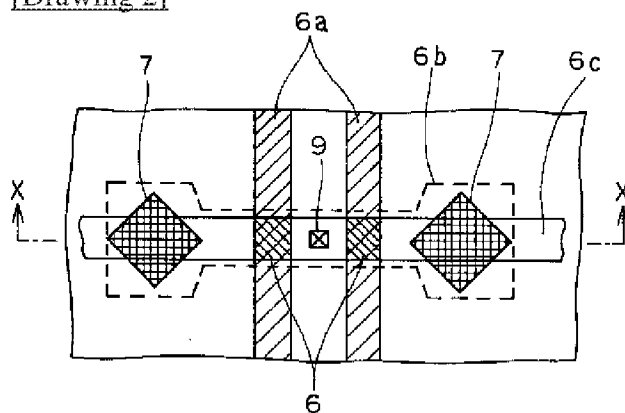
6b Active region

6c, 19 bit lines
 7 and 20 Slot type capacitor
 7 g Capacitor oxide film
 7h capacitor electrode
 8, 11 field oxide
 9 Contact hole
 11 Cross line
 13 Source
 14 and 26 Drain
 15 Interlayer insulation film
 The identical codes in a figure show a same or considerable portion.

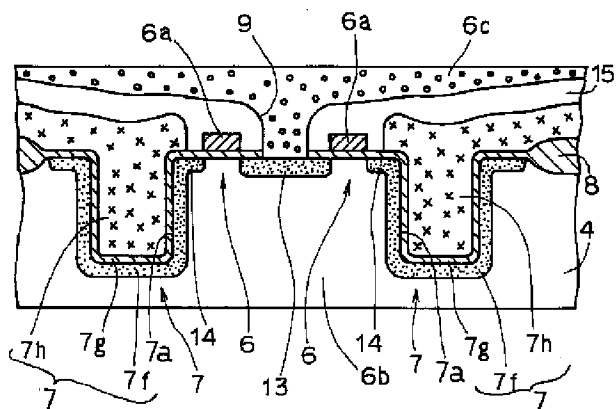
[Drawing 1]



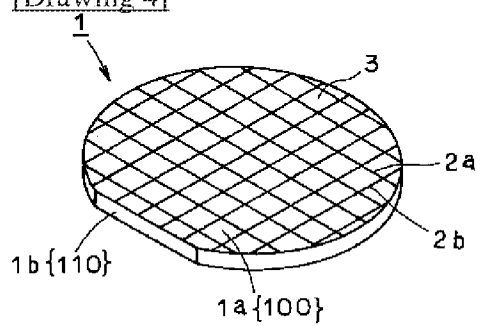
[Drawing 2]



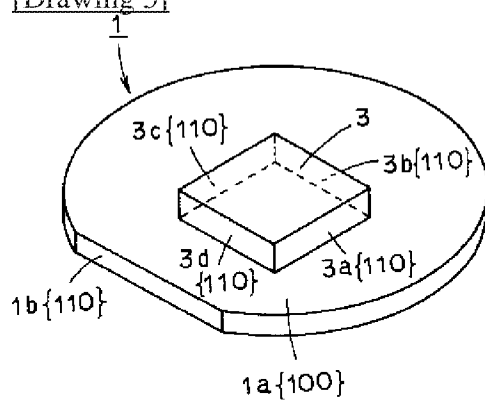
[Drawing 3]



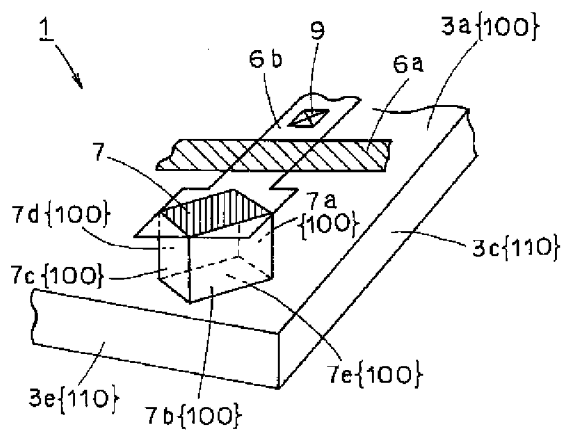
[Drawing 4]



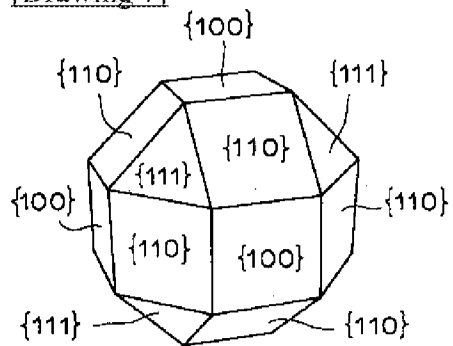
[Drawing 5]



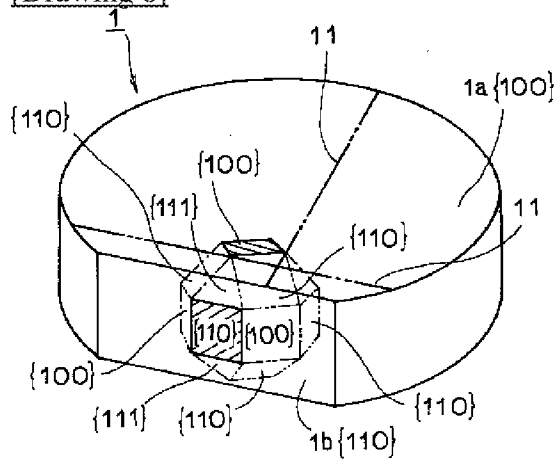
[Drawing 6]



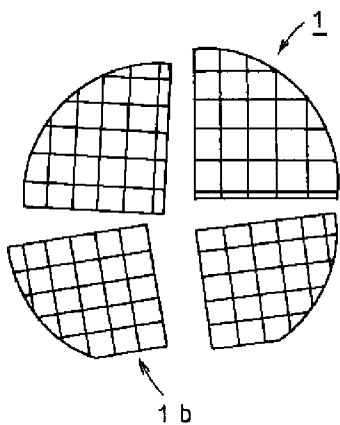
[Drawing 7]



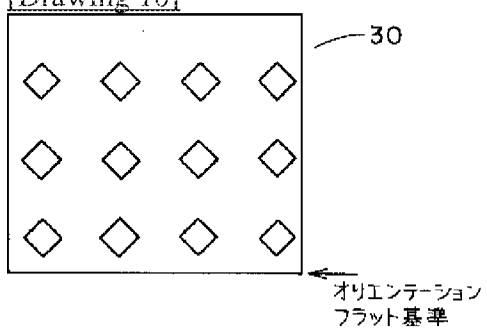
[Drawing 8]



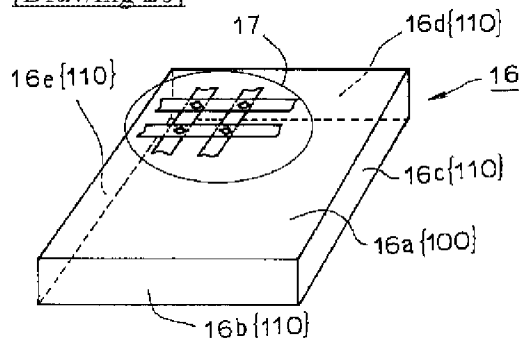
[Drawing 9]



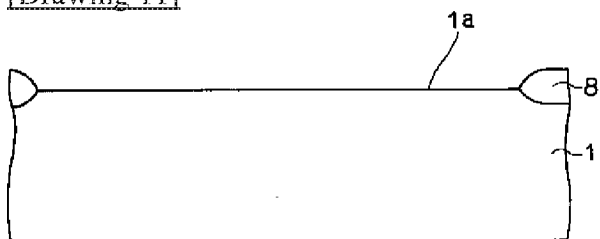
[Drawing 10]



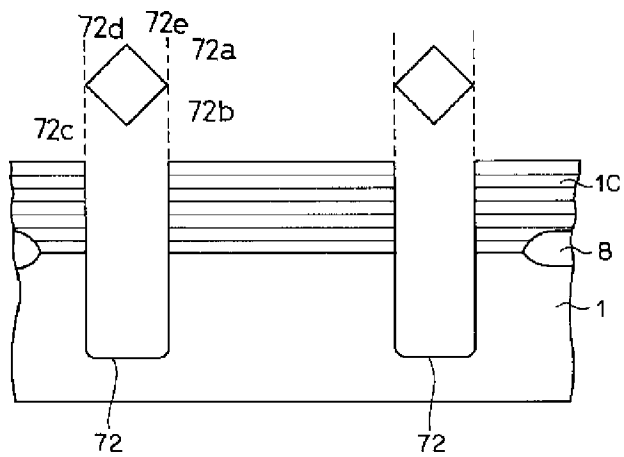
[Drawing 20]



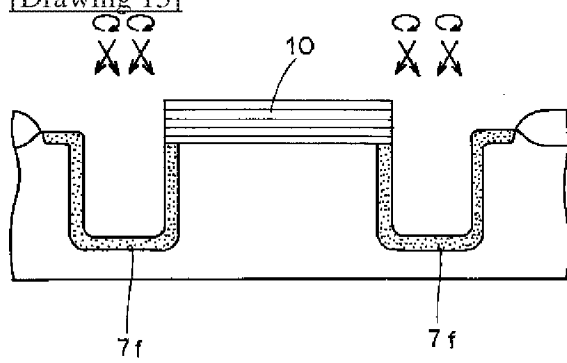
[Drawing 11]



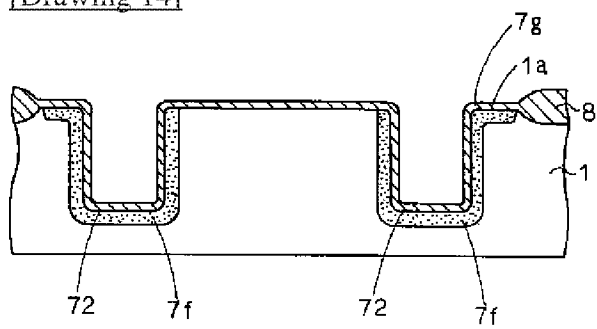
[Drawing 12]



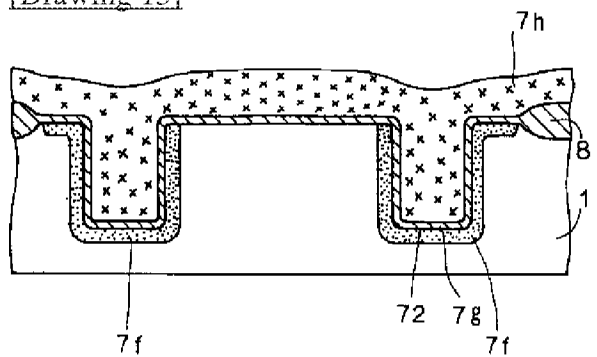
[Drawing 13]



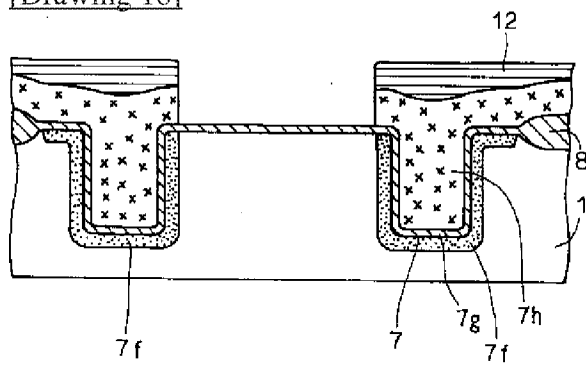
[Drawing 14]



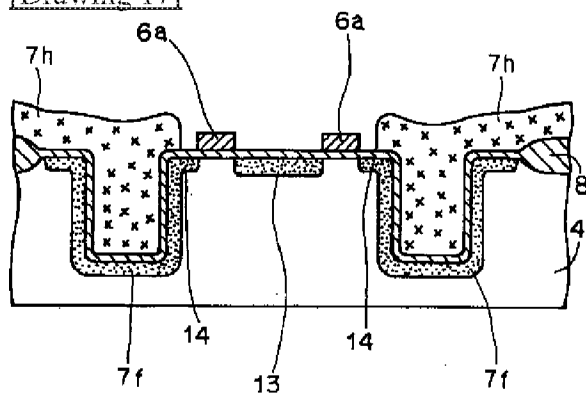
[Drawing 15]



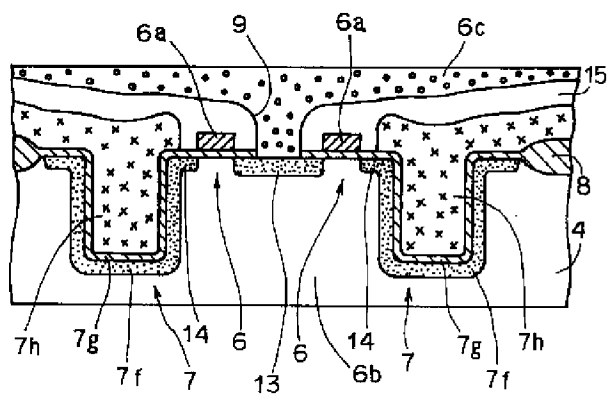
[Drawing 16]



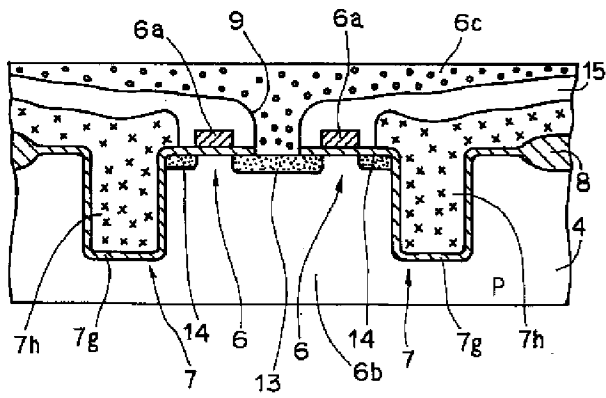
[Drawing 17]



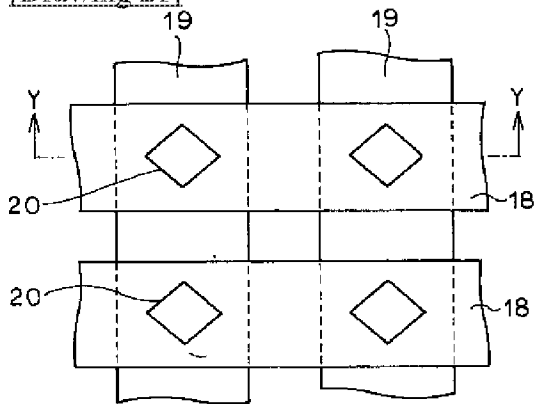
[Drawing 18]



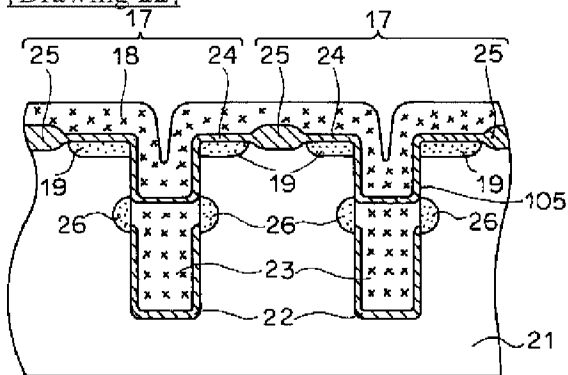
[Drawing 19]



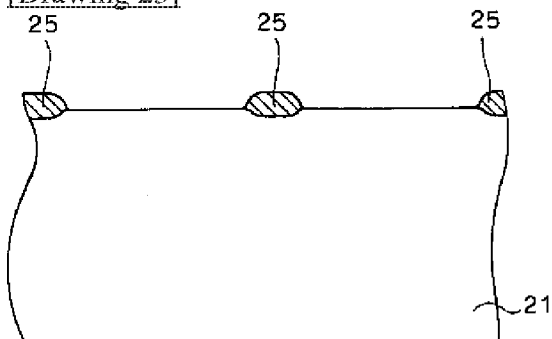
[Drawing 21]



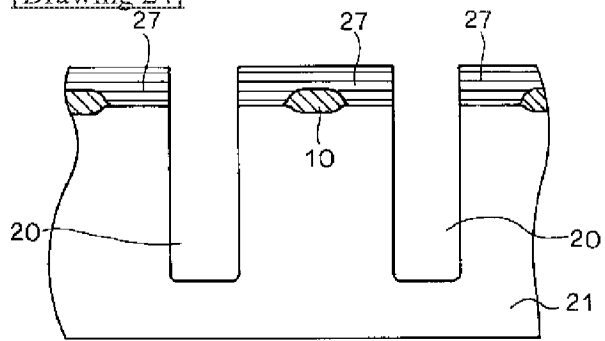
[Drawing 22]



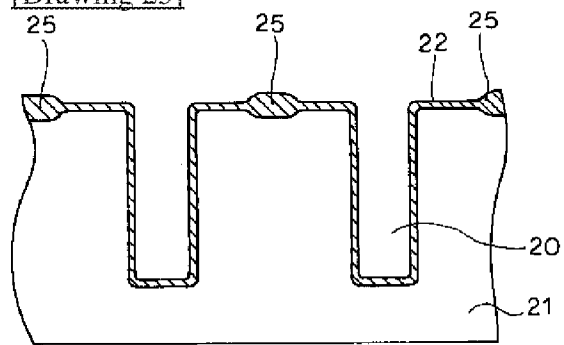
[Drawing 23]



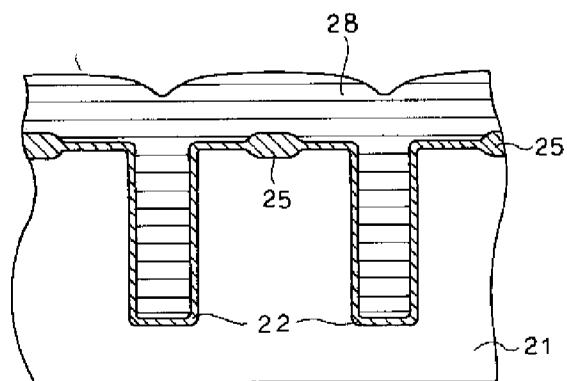
[Drawing 24]



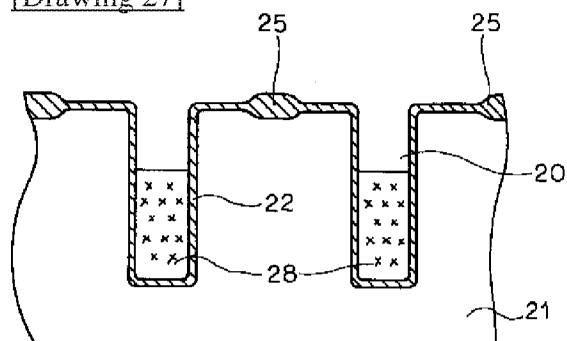
[Drawing 25]



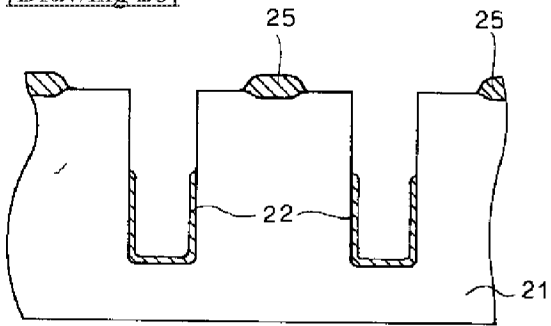
[Drawing 26]



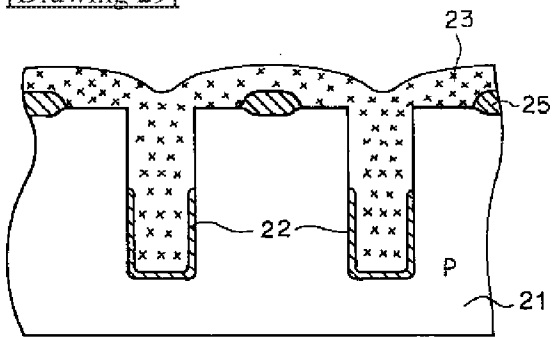
[Drawing 27]



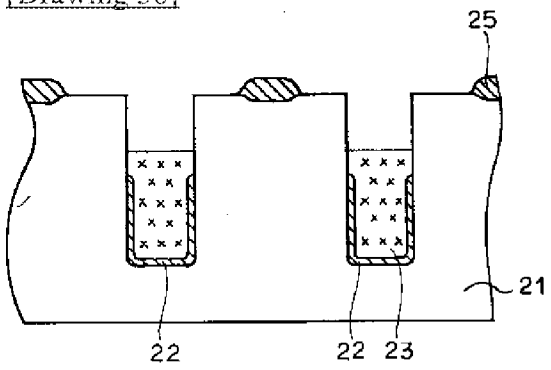
[Drawing 28]



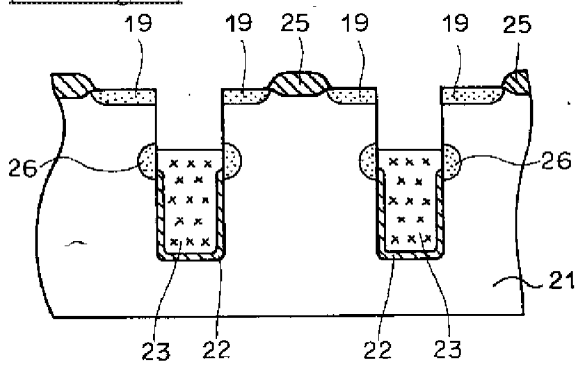
[Drawing 29]



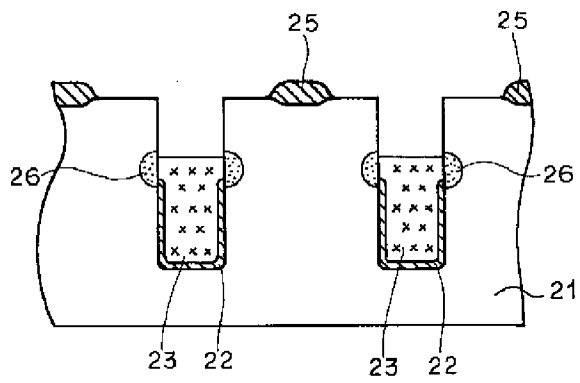
[Drawing 30]



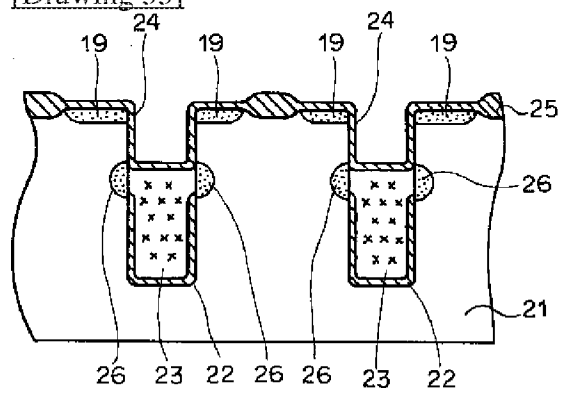
[Drawing 32]



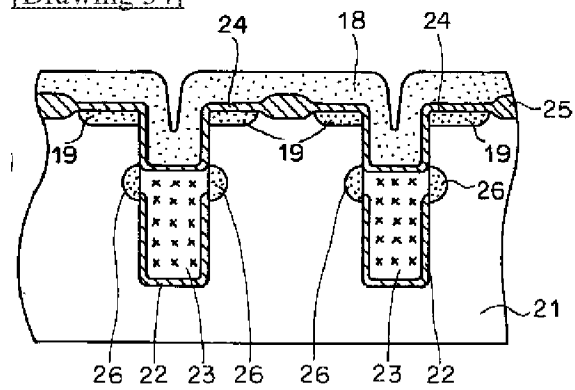
[Drawing 31]



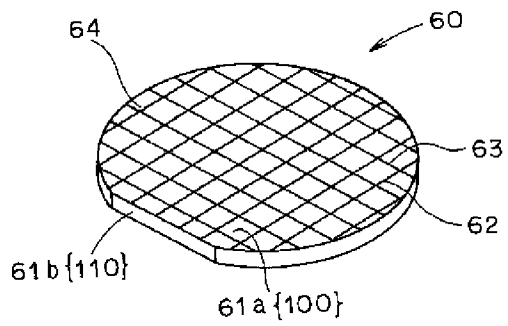
[Drawing 33]



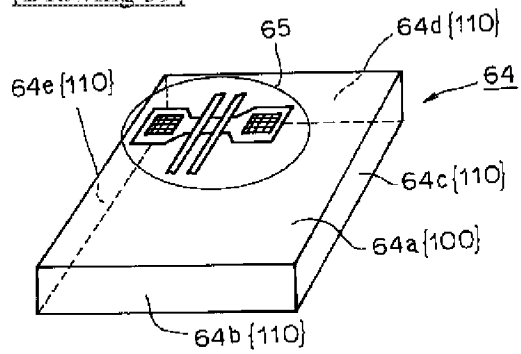
[Drawing 34]



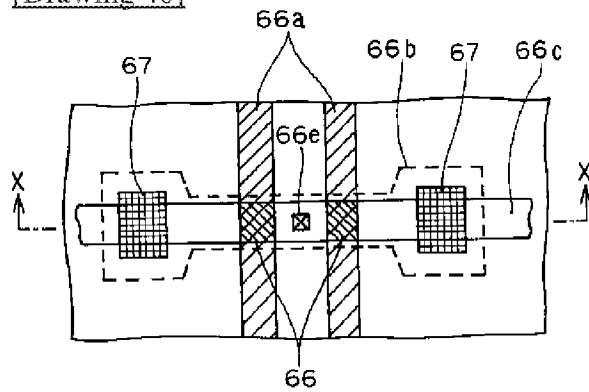
[Drawing 35]



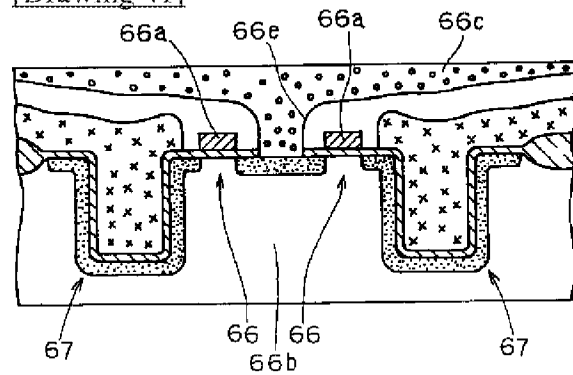
[Drawing 39]



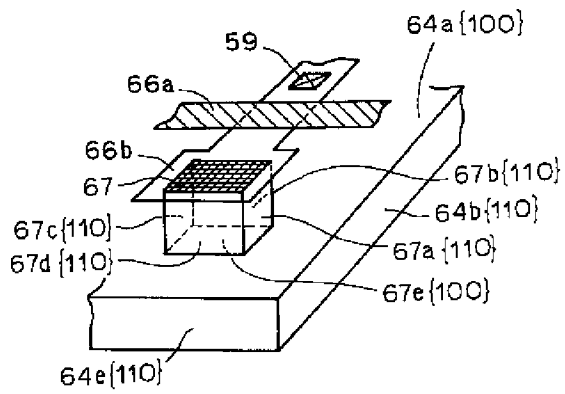
[Drawing 40]



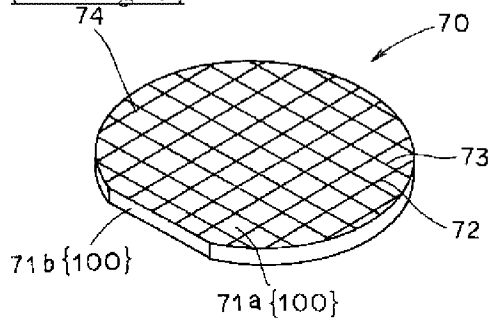
[Drawing 41]



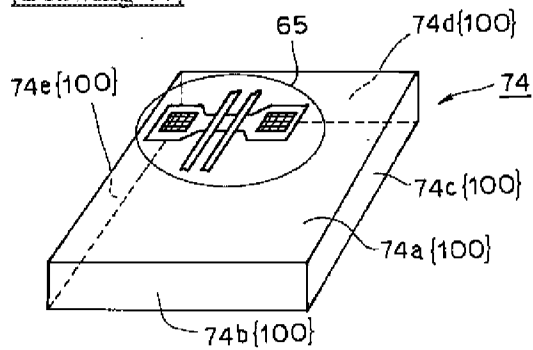
[Drawing 42]



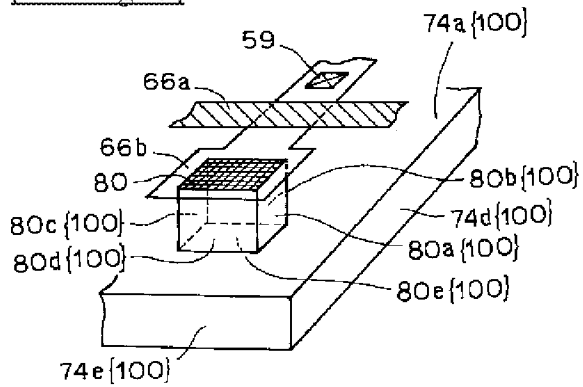
[Drawing 43]



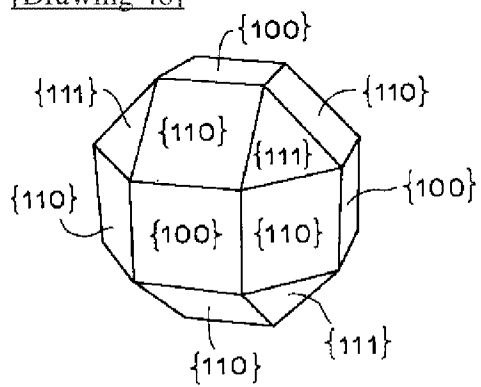
[Drawing 44]



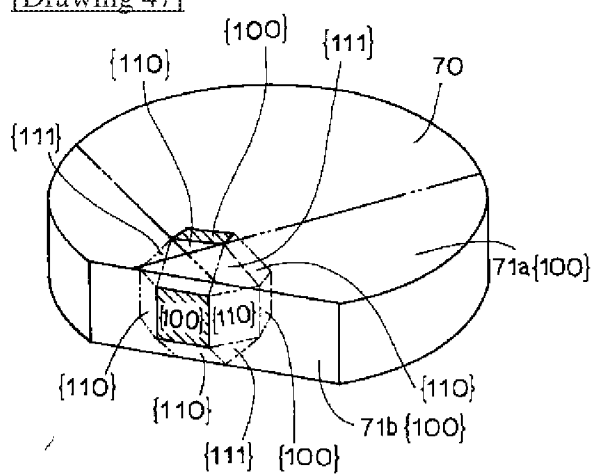
[Drawing 45]



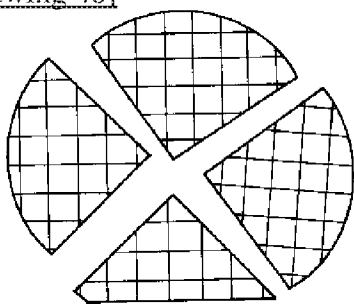
[Drawing 46]



[Drawing 47]



[Drawing 48]



[Translation done.]